**Cairo University Faculty of Engineering**

**Advanced Topics in Electronics-1**

**Under supervision of:**

**Dr. Mohamed Youssef**

**Eng. Ahmed Atef**

**Students Names:**

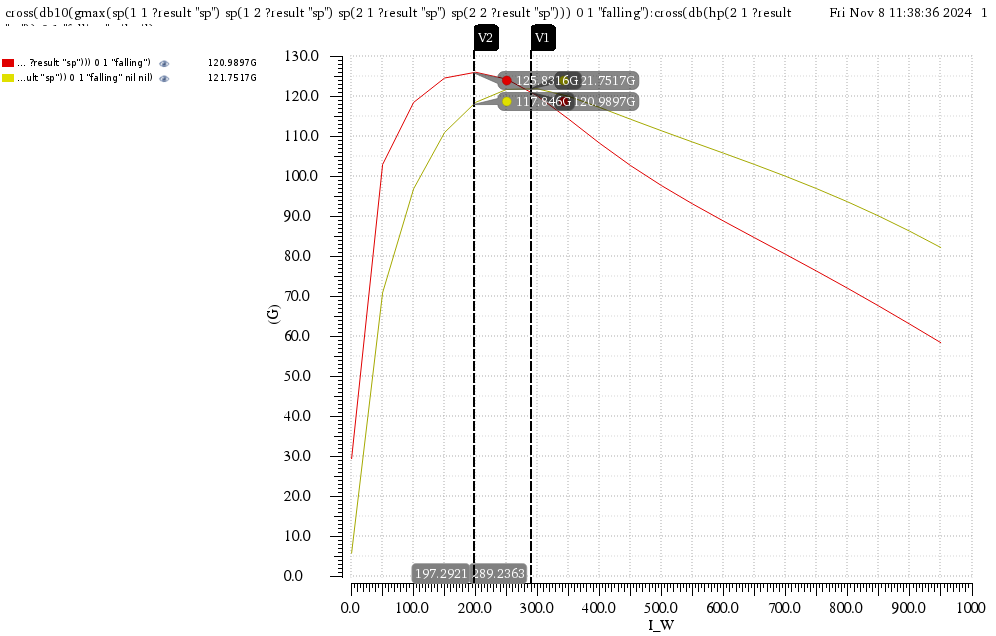
**Kerolos Hanna Fayez 1200049**

**Omar Mohamed Said 1200859**

1. & versus current density for . Find

**NMOS:**

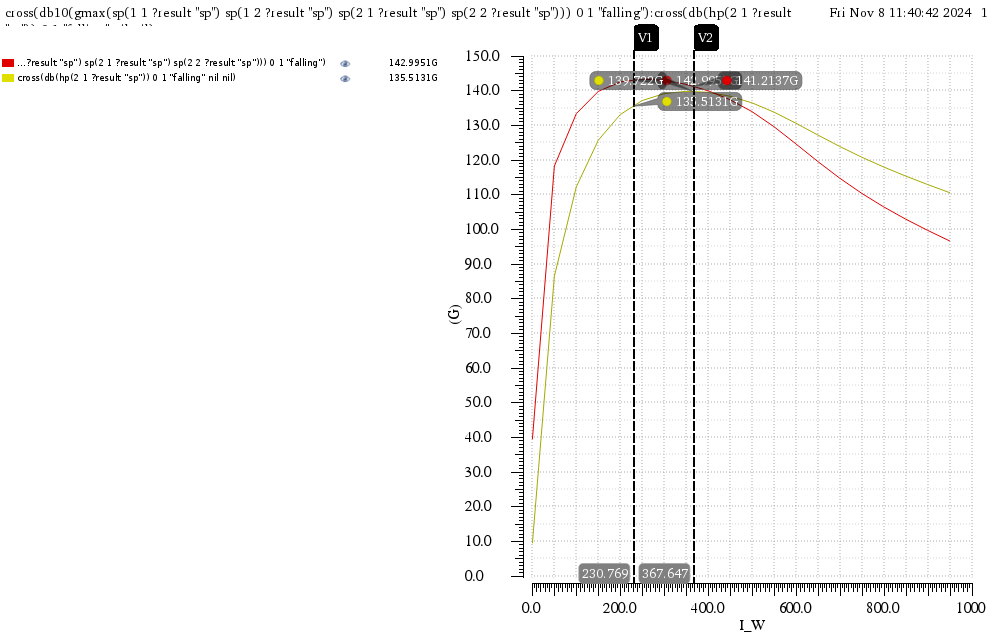
At



with highest

with highest

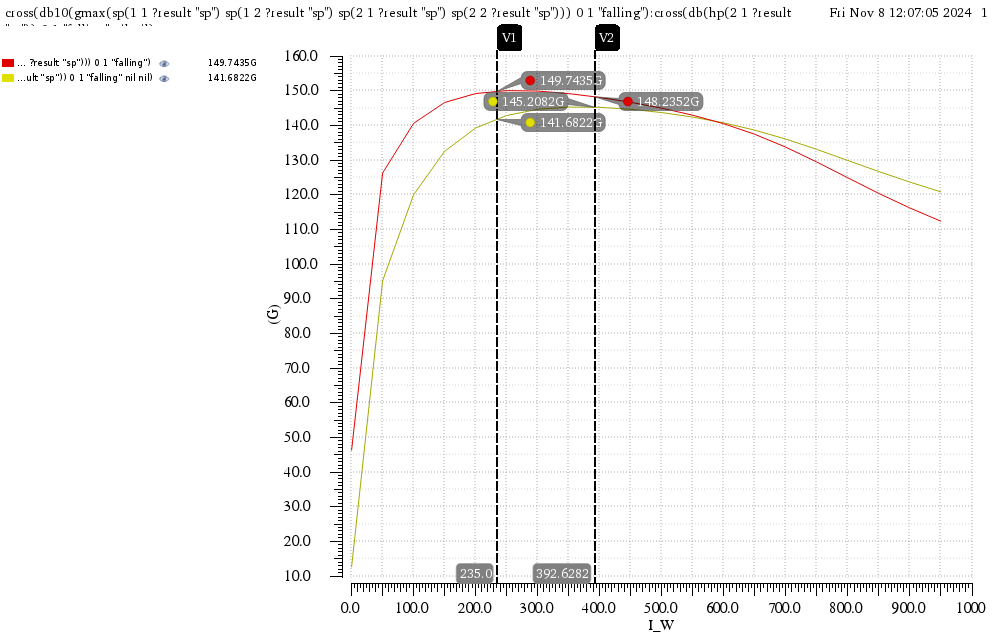
At :



with highest

with highest

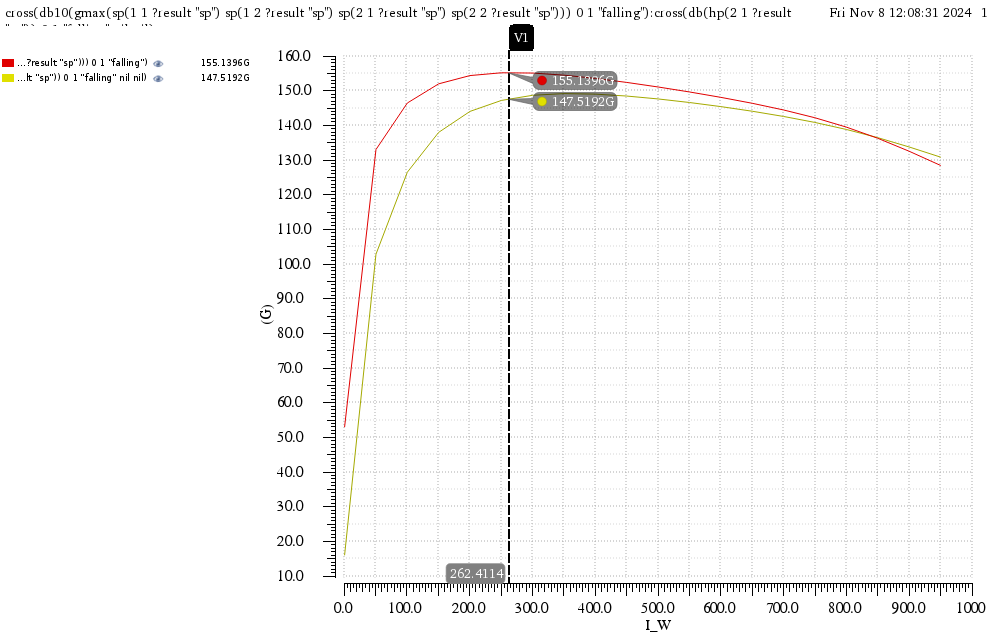
At :



with highest

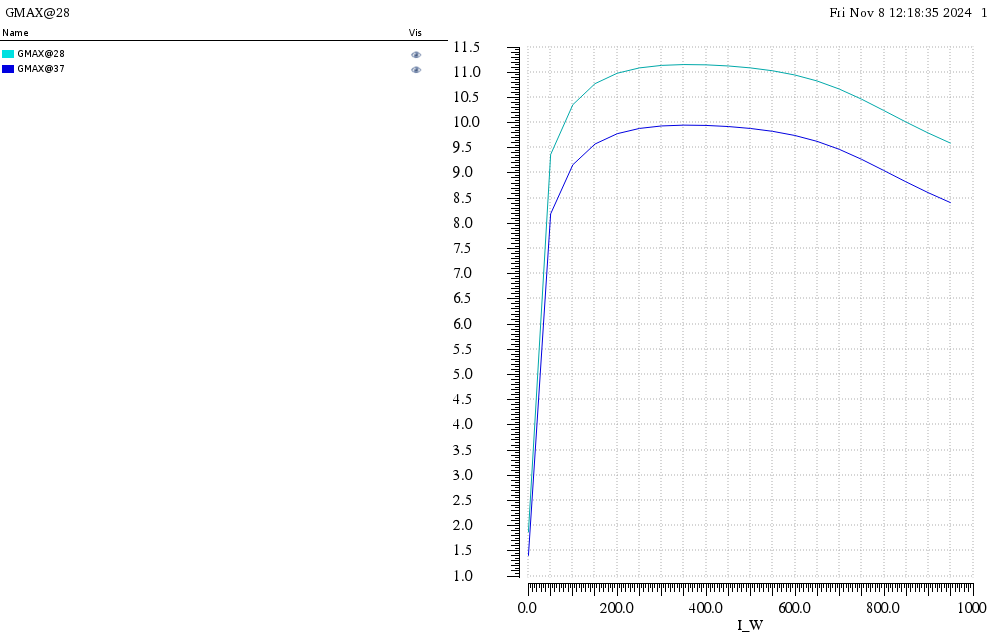
with highest

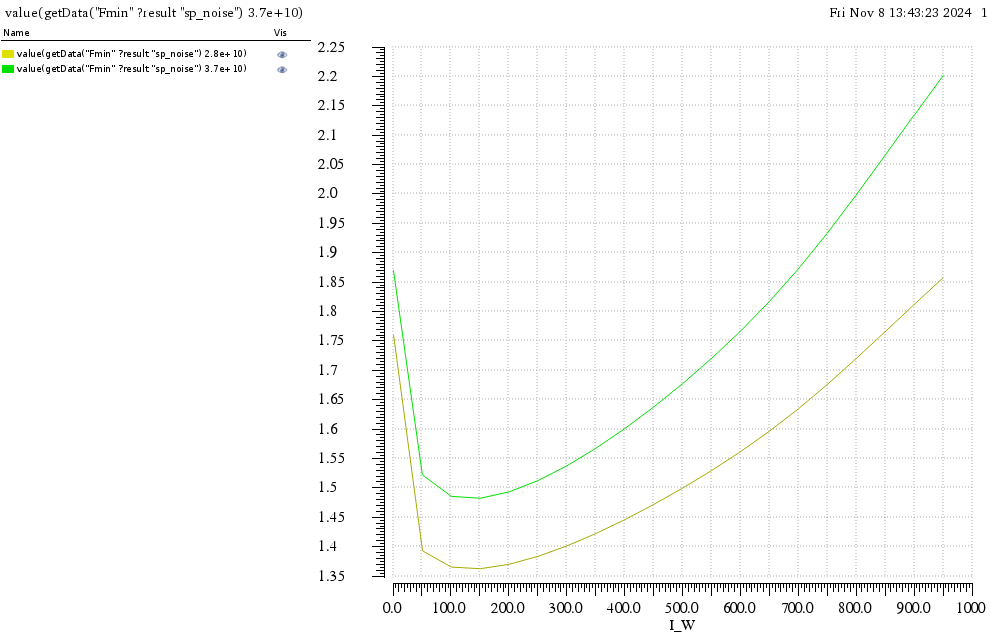
At :



with highest

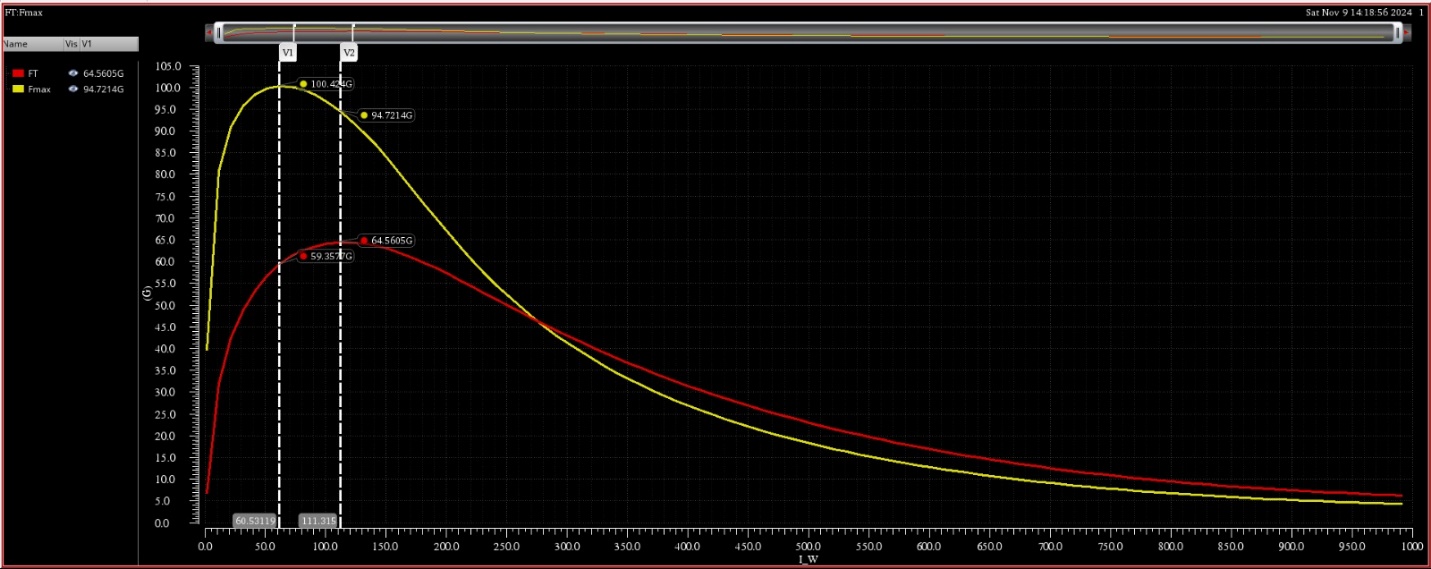
with highest





**PMOS:**

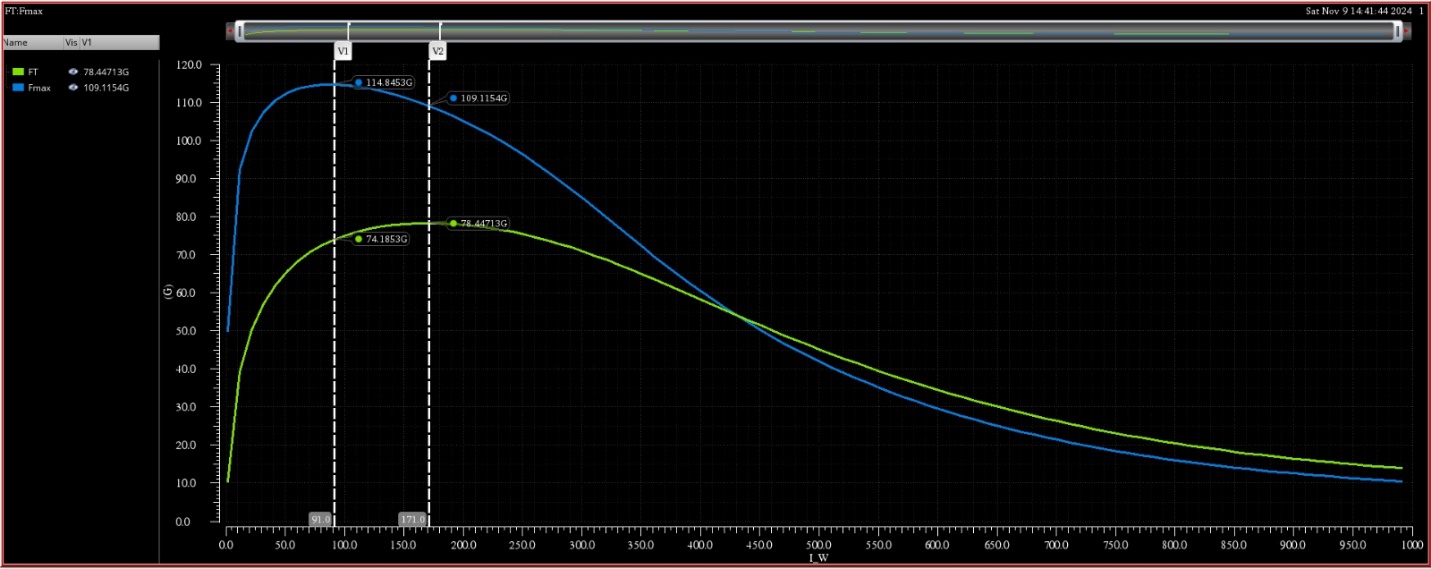
At



with highest

with highest

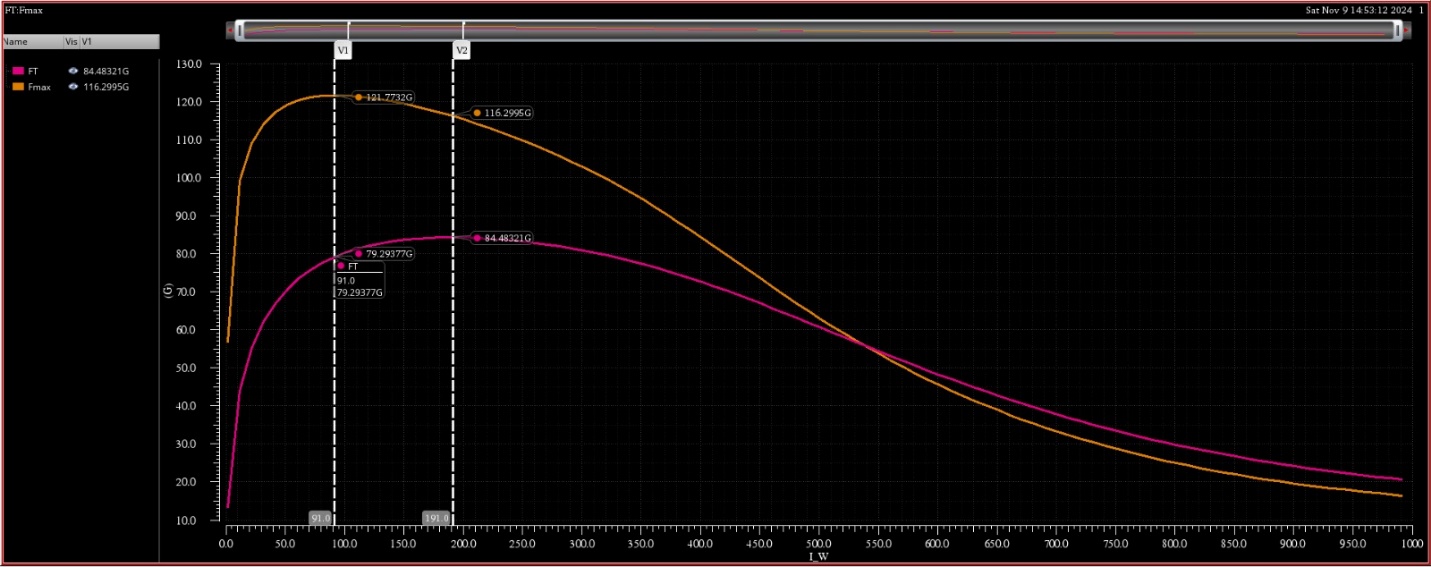
At



with highest

with highest

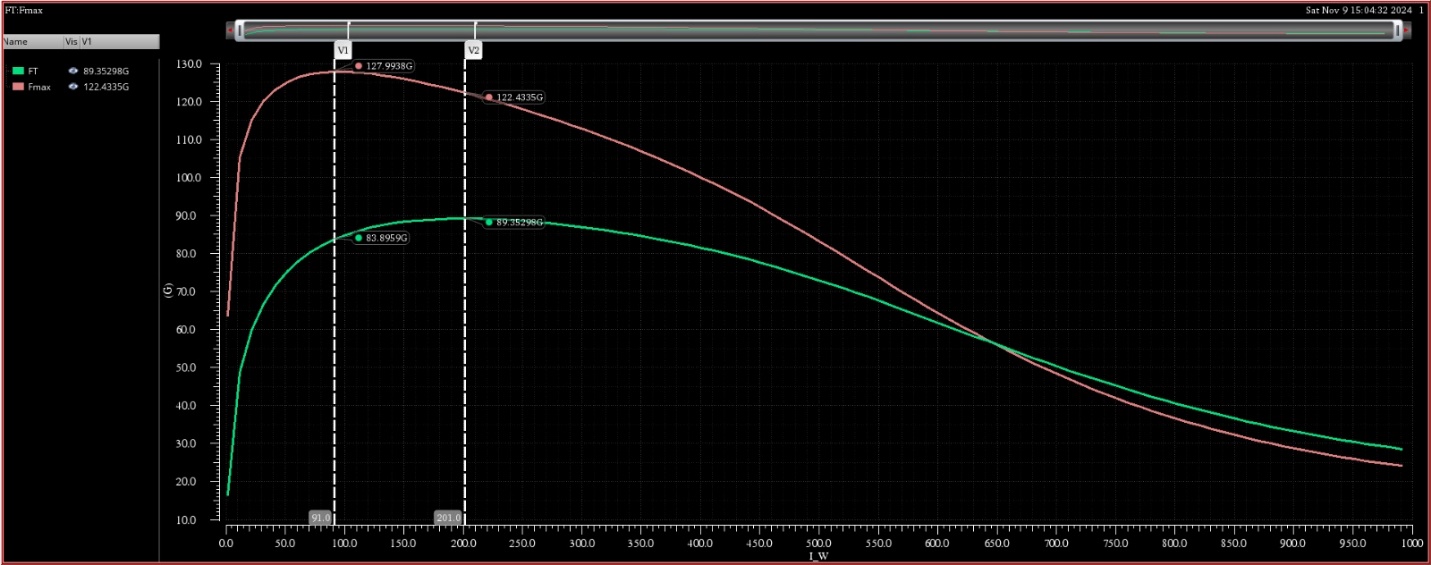
At



with highest

with highest

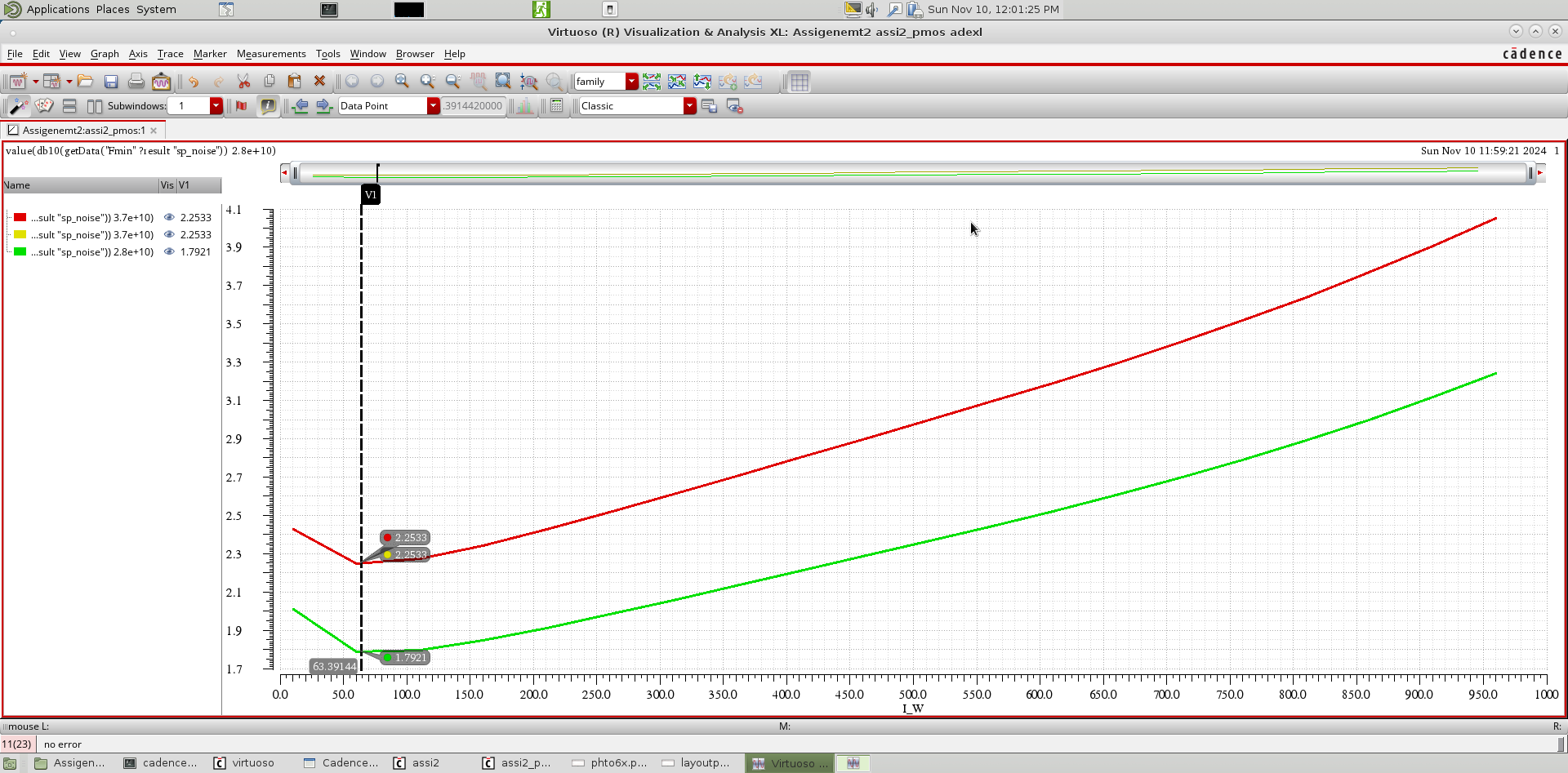
At



with highest

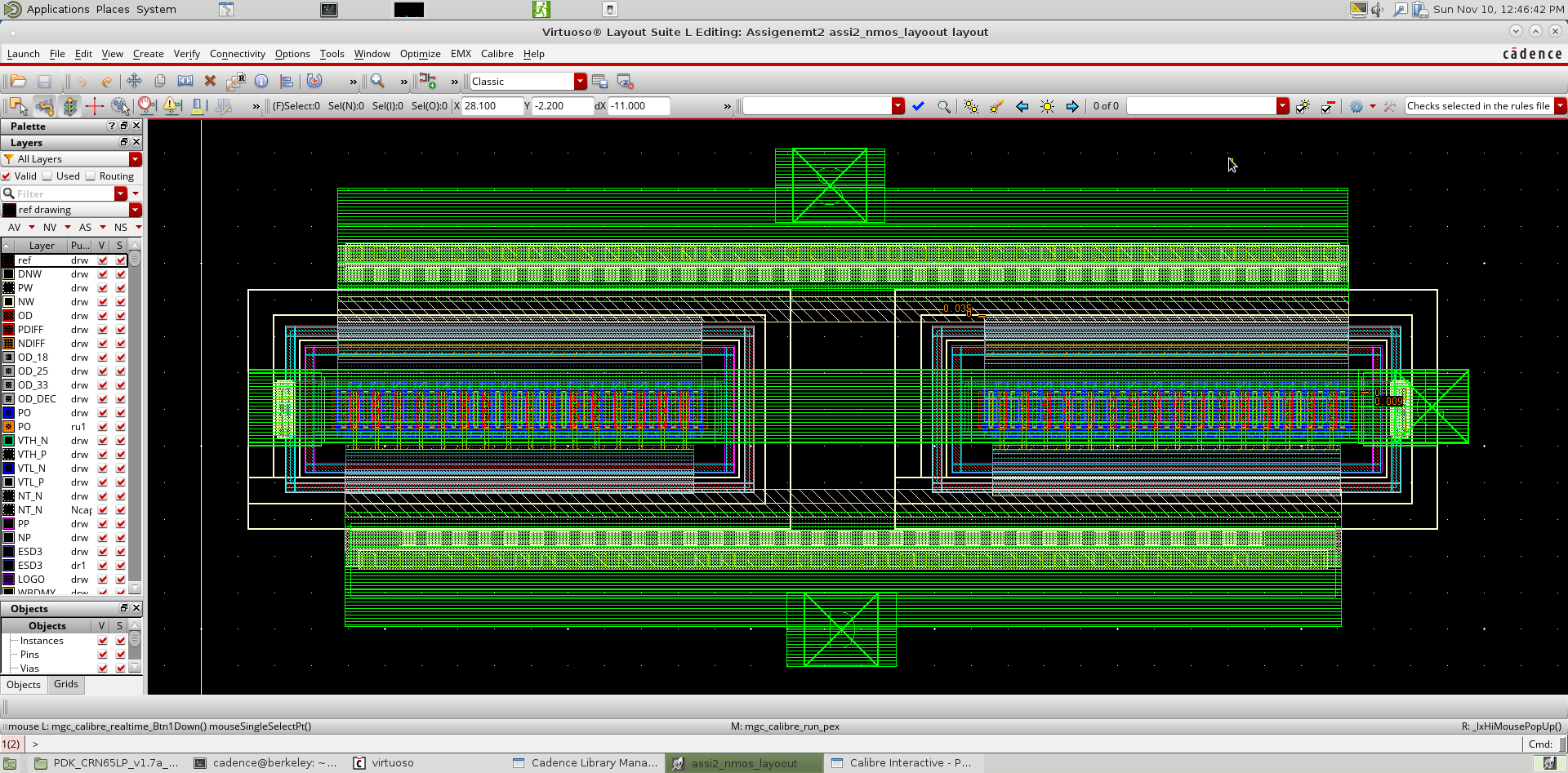
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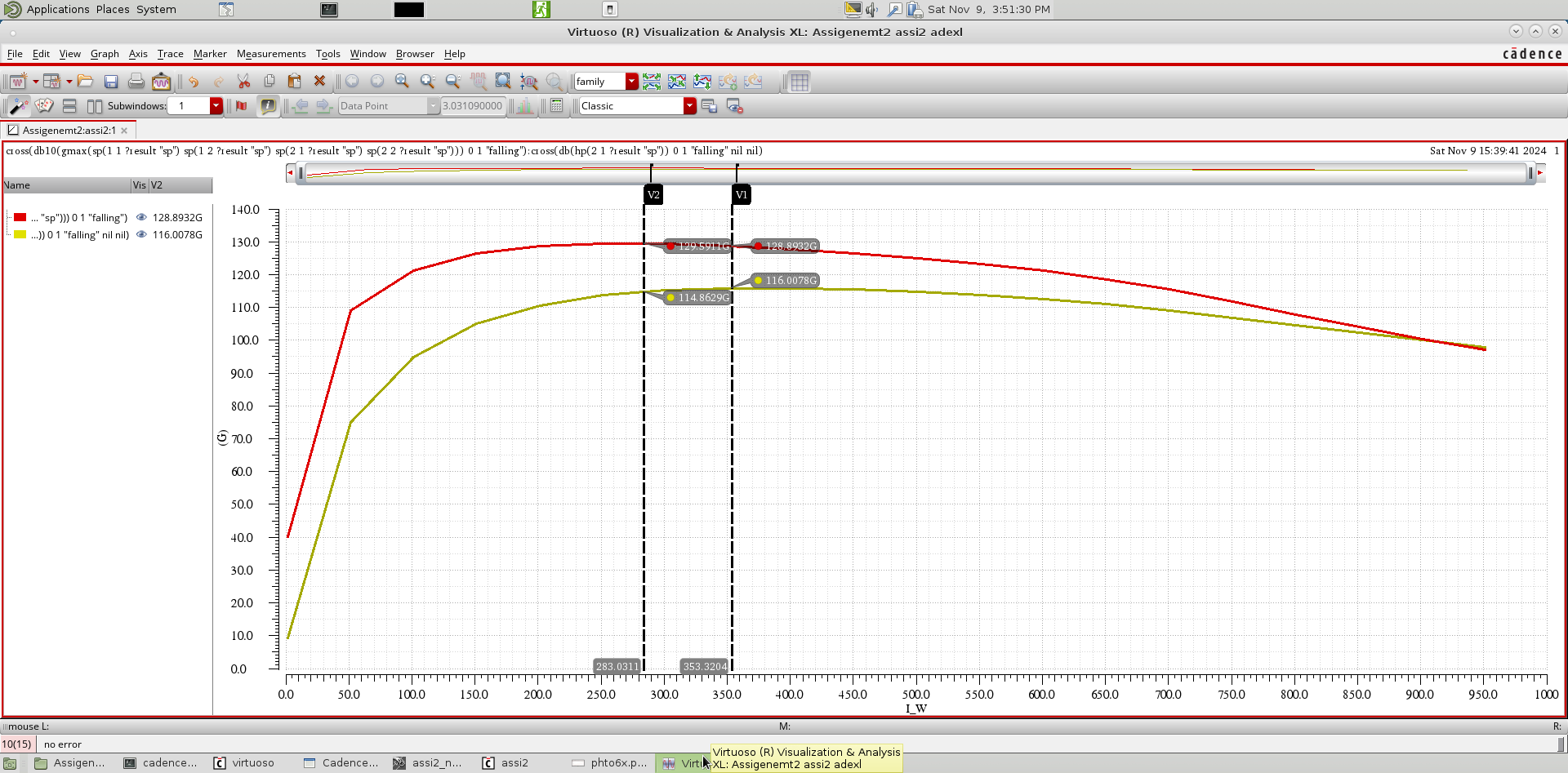




4. Repeat 1 to 3 after running RC extraction for the devices (make sure all the parasitics up to the top metallization with the routing of the 2 multipliers are included) and replot on the same graphs only for

**NMOS layout**





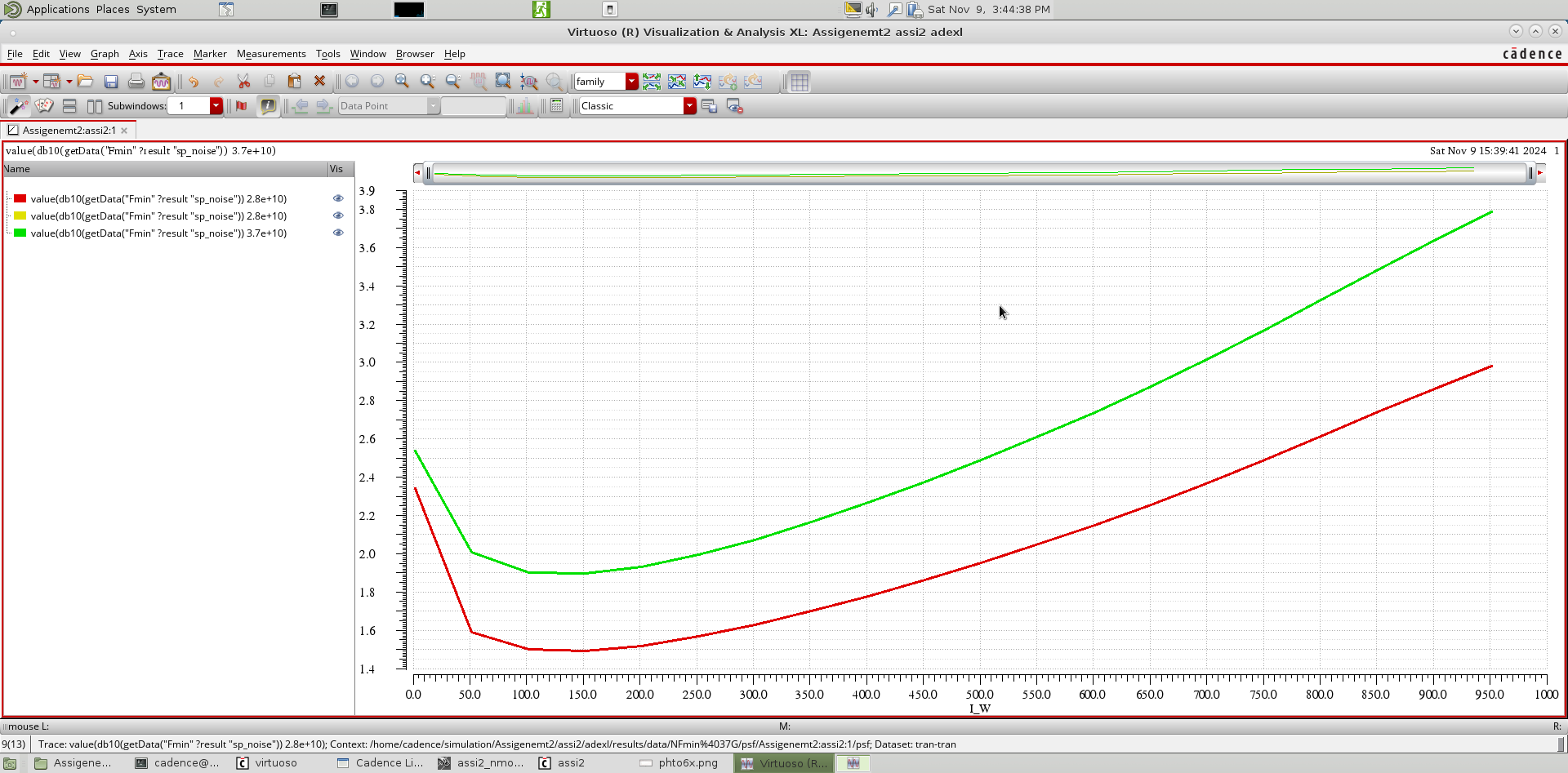
with highest

with highest

The value of and degrade because of parasitic generated by layout.

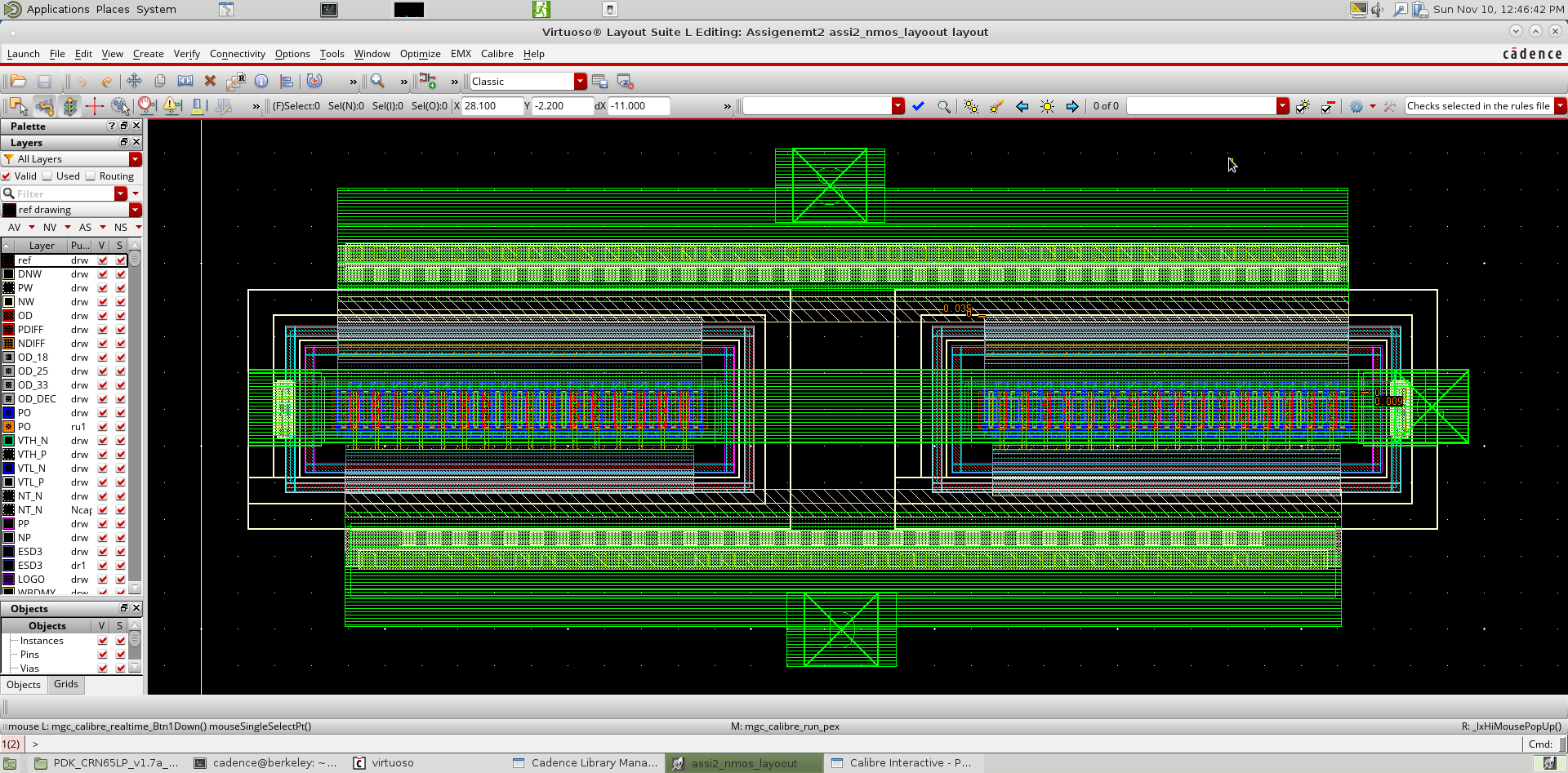
Before layout at . was equal to &

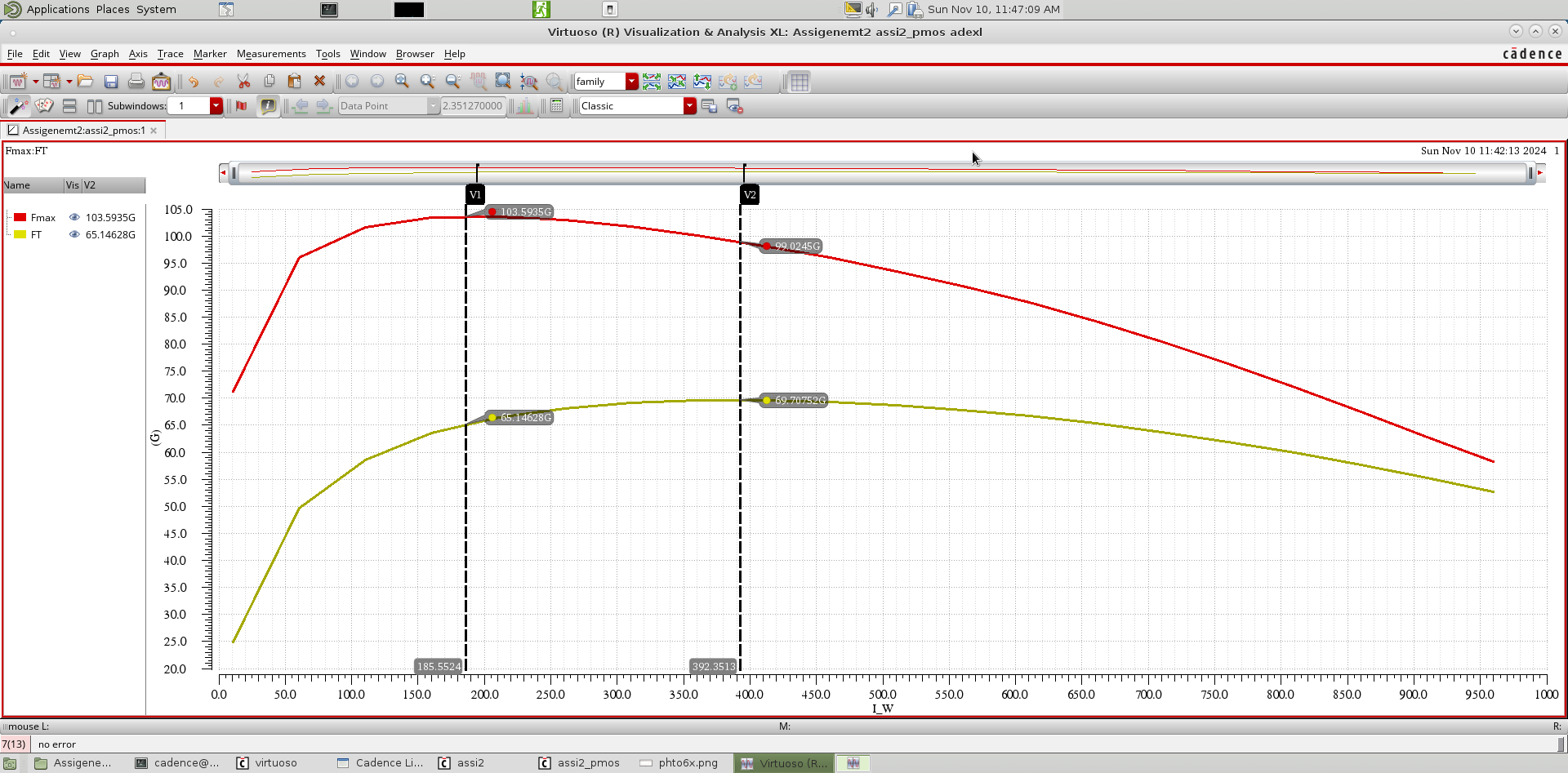




We can also see that the noise figure increased due to parasetics.

**PMOS layout**



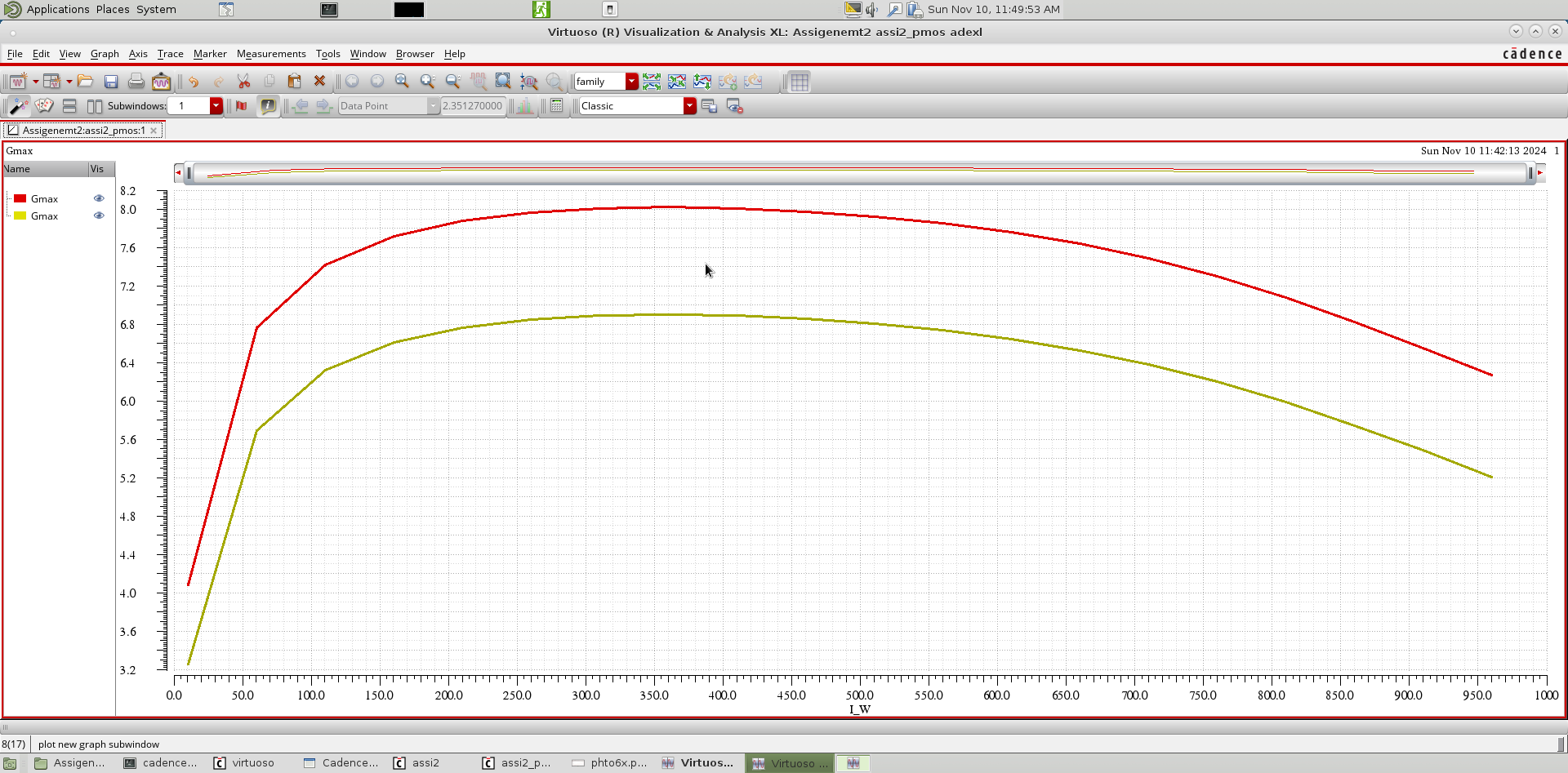


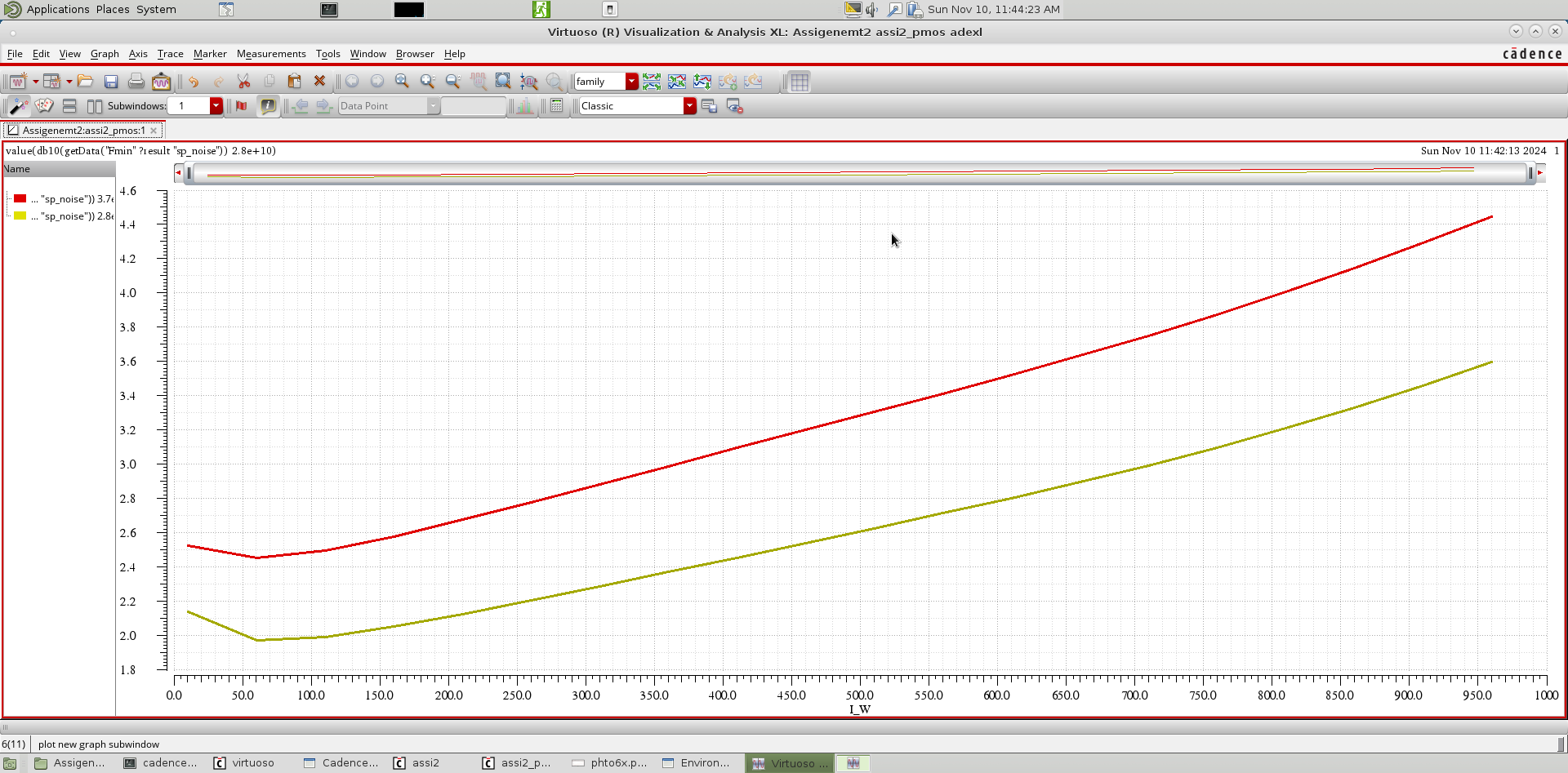
with highest

with highest

The value of and degrade because of parasitic generated by layout.

Before layout at . &

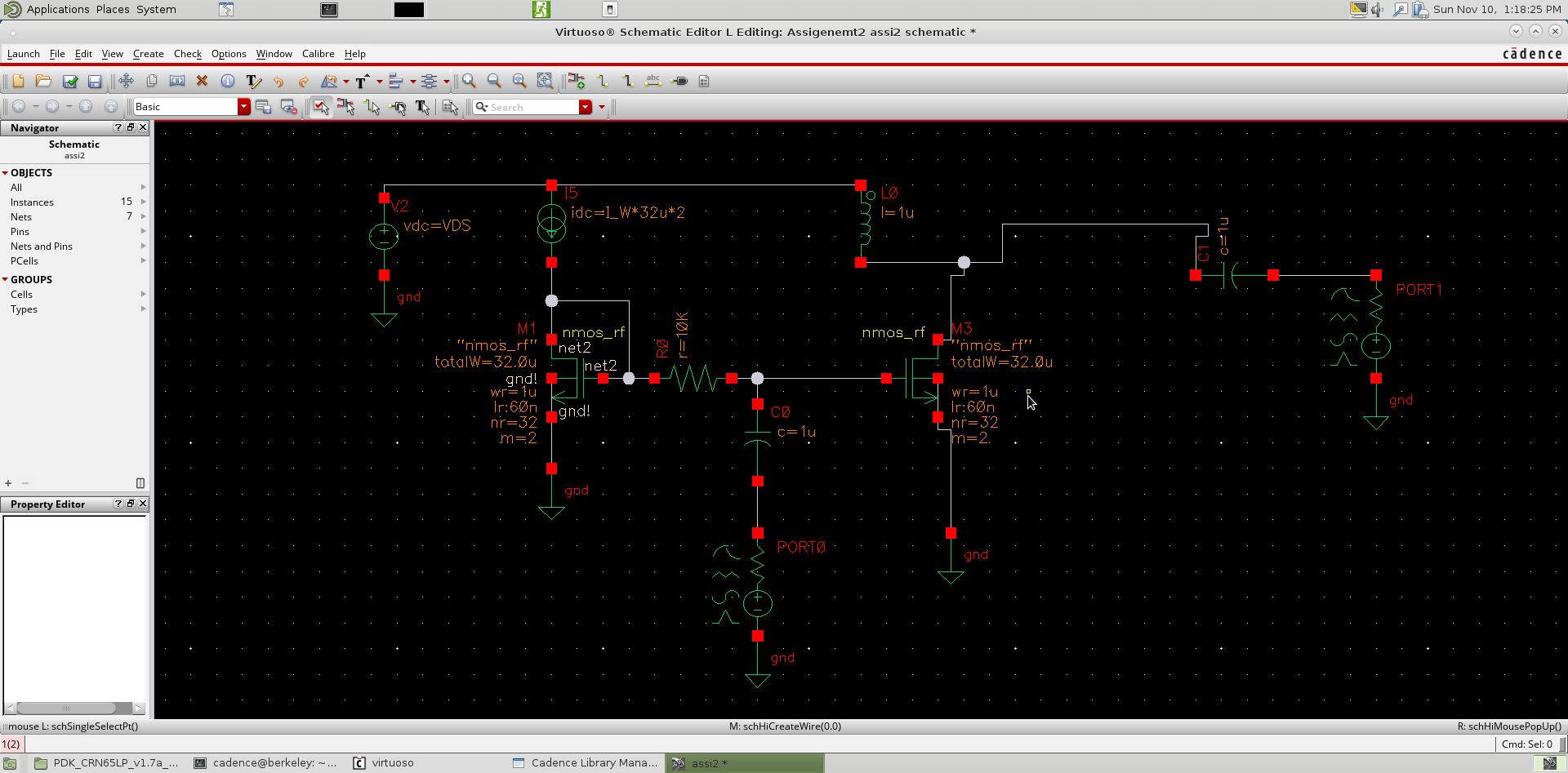


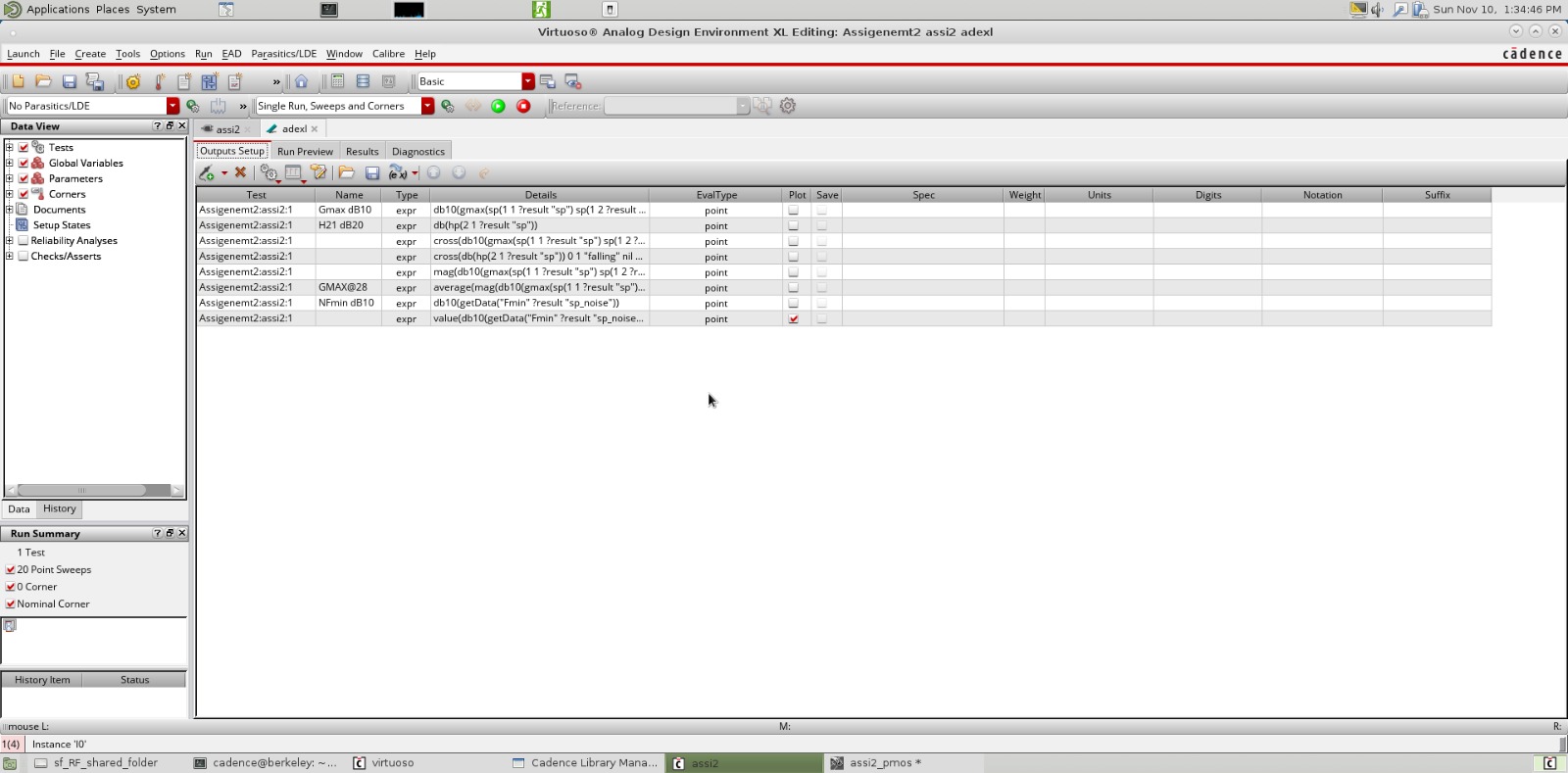


We can also see that the noise figure increased due to parasetics.

5. Show the testbench used to generate the results

**NMOS testbench:**





**PMOS testbench:**

